

FIG. 1
(PRIOR ART)

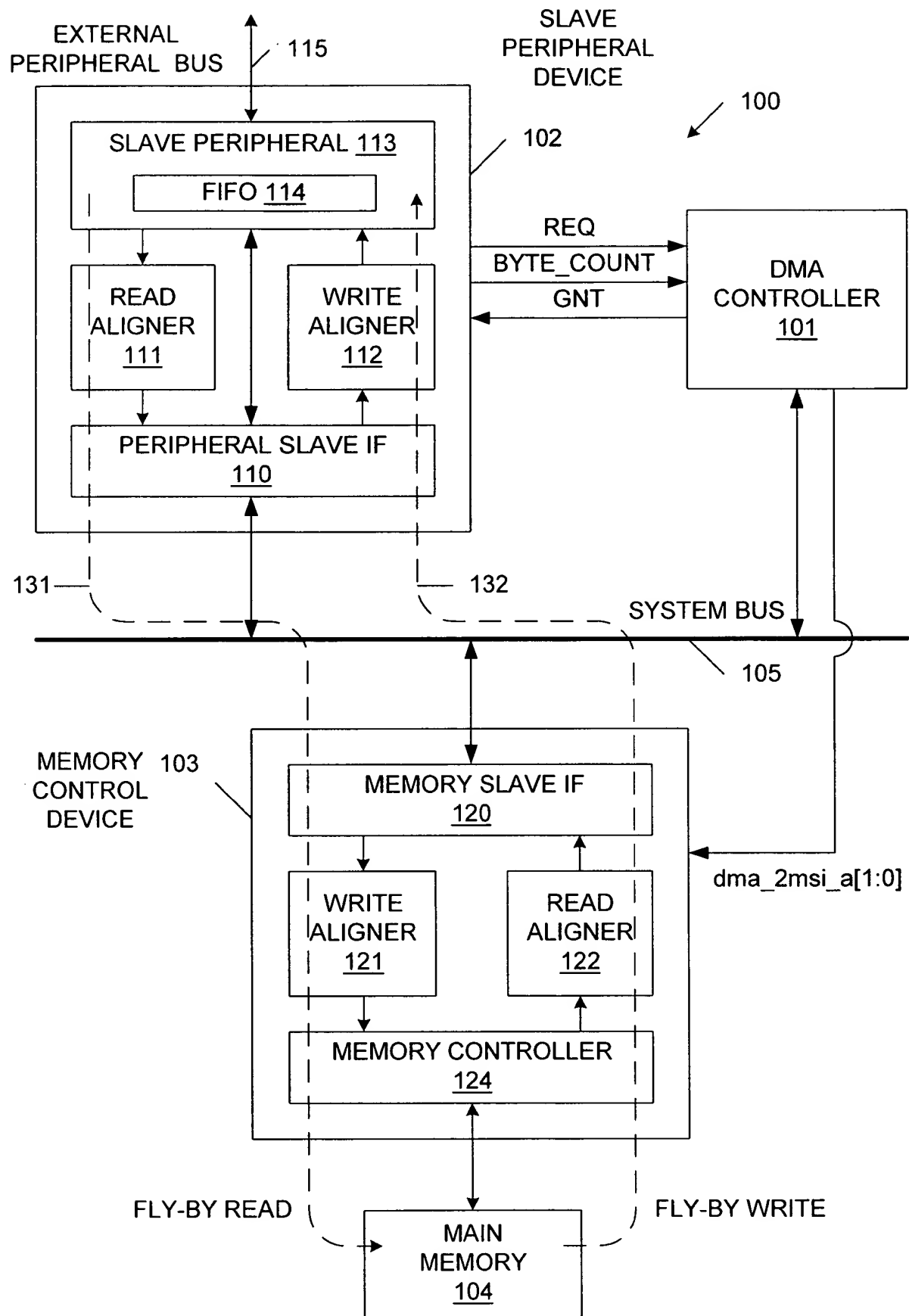


FIG. 2

DATA IN FIFO 114

	00	01	10	11
201	x	x	A	B
202	C	D	E	F
203	G	H	I	J
204	K	L	M	N
205	O	P	Q	R
206	S	T	U	V
207	W	X	Y	Z

⋮

114

FIG. 3

DATA ON SYSTEM BUS 105

	00	01	10	11
301	A	B	C	D
302	E	F	G	H
303	I	J	K	L
304	M	N	O	P
305	Q	R	S	T
306	U	V	W	X
307	Y	Z	x	x

105

FIG. 4

DATA TO MEMORY 104

	00	01	10	11
401	x	x	x	A
402	B	C	D	E
403	F	G	H	I
404	J	K	L	M
405	N	O	P	Q
406	R	S	T	U
407	V	W	X	Y
408	Z	x	x	x

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FIG. 5

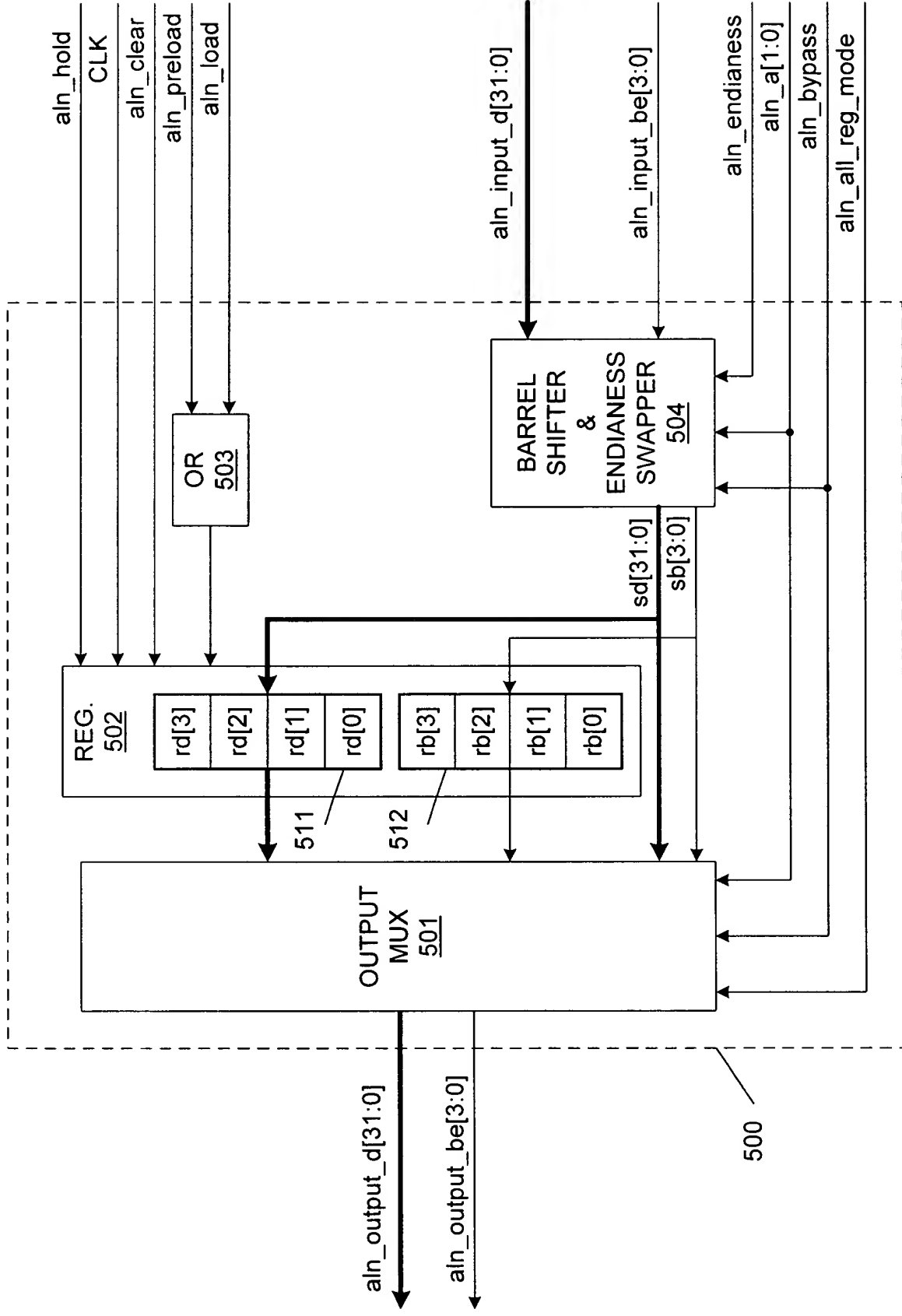


FIG. 6

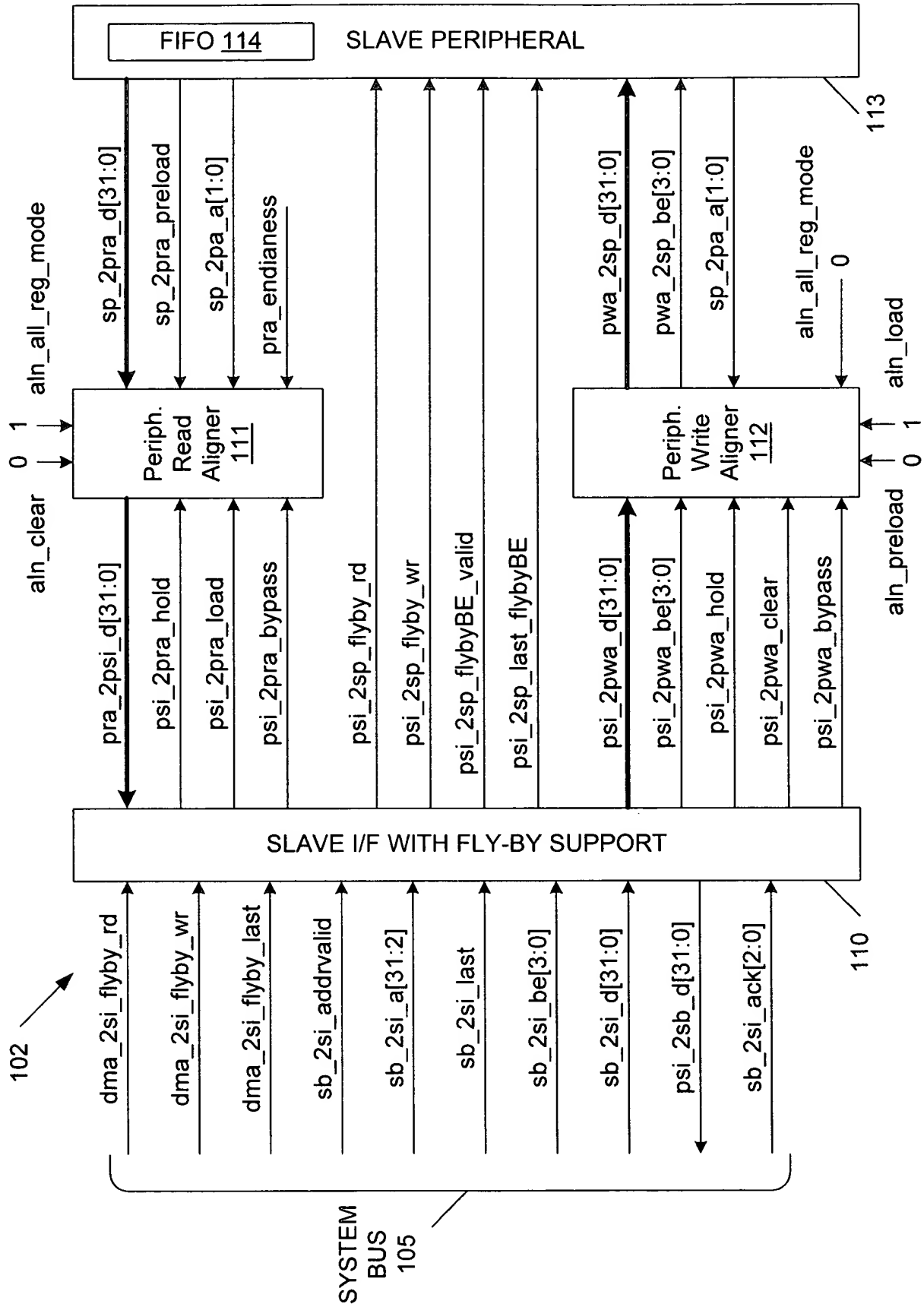


FIG. 7

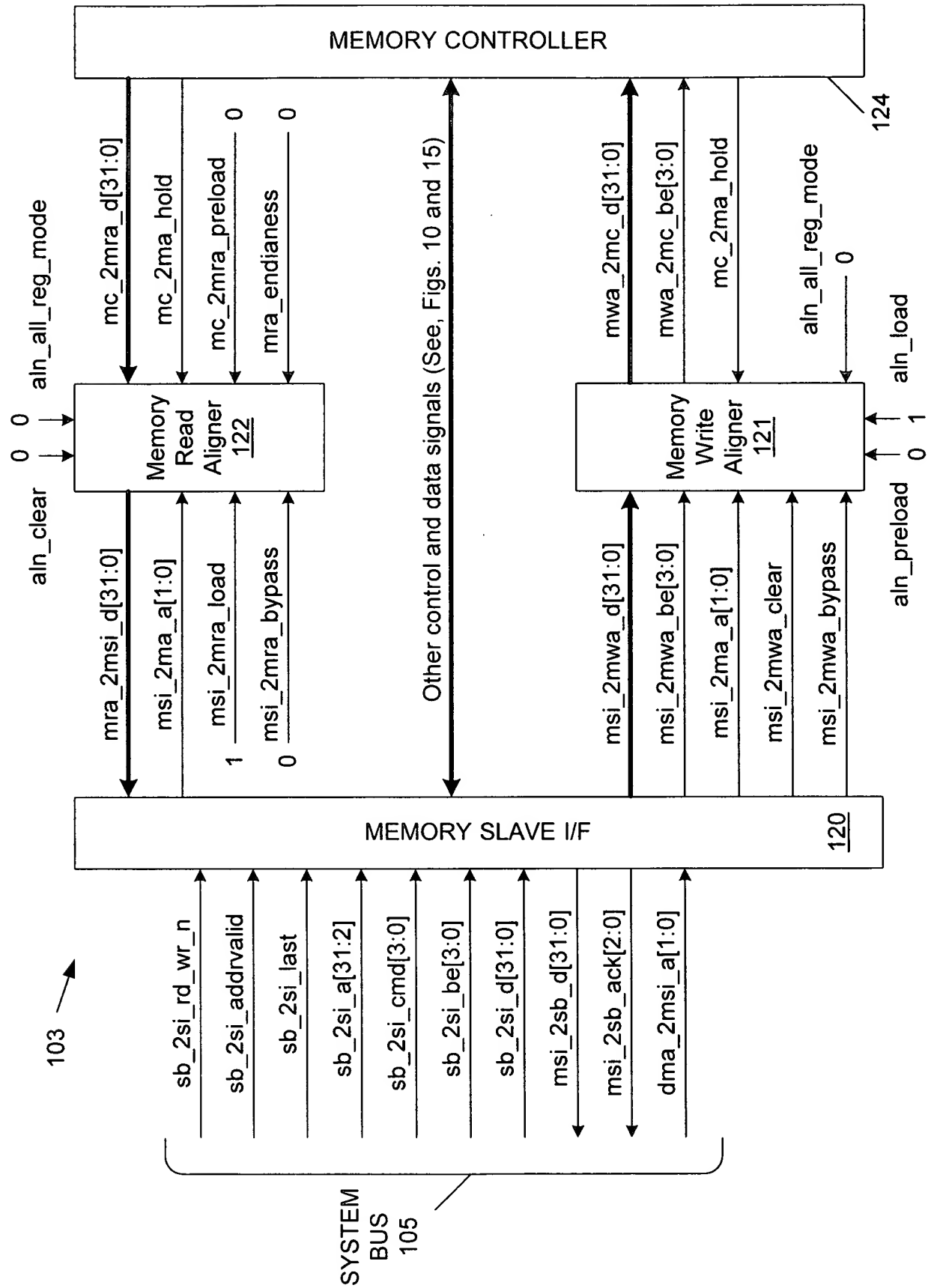
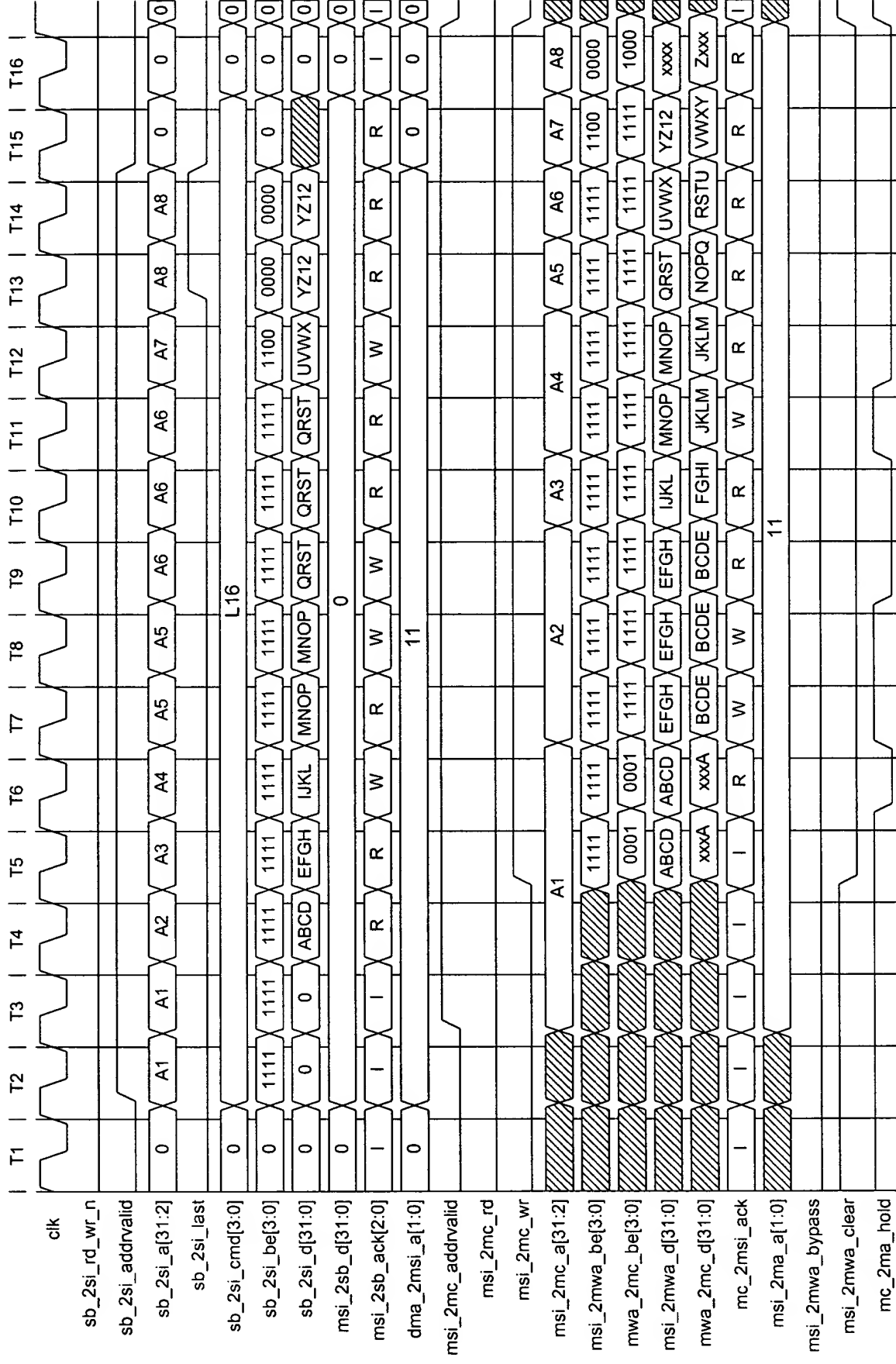
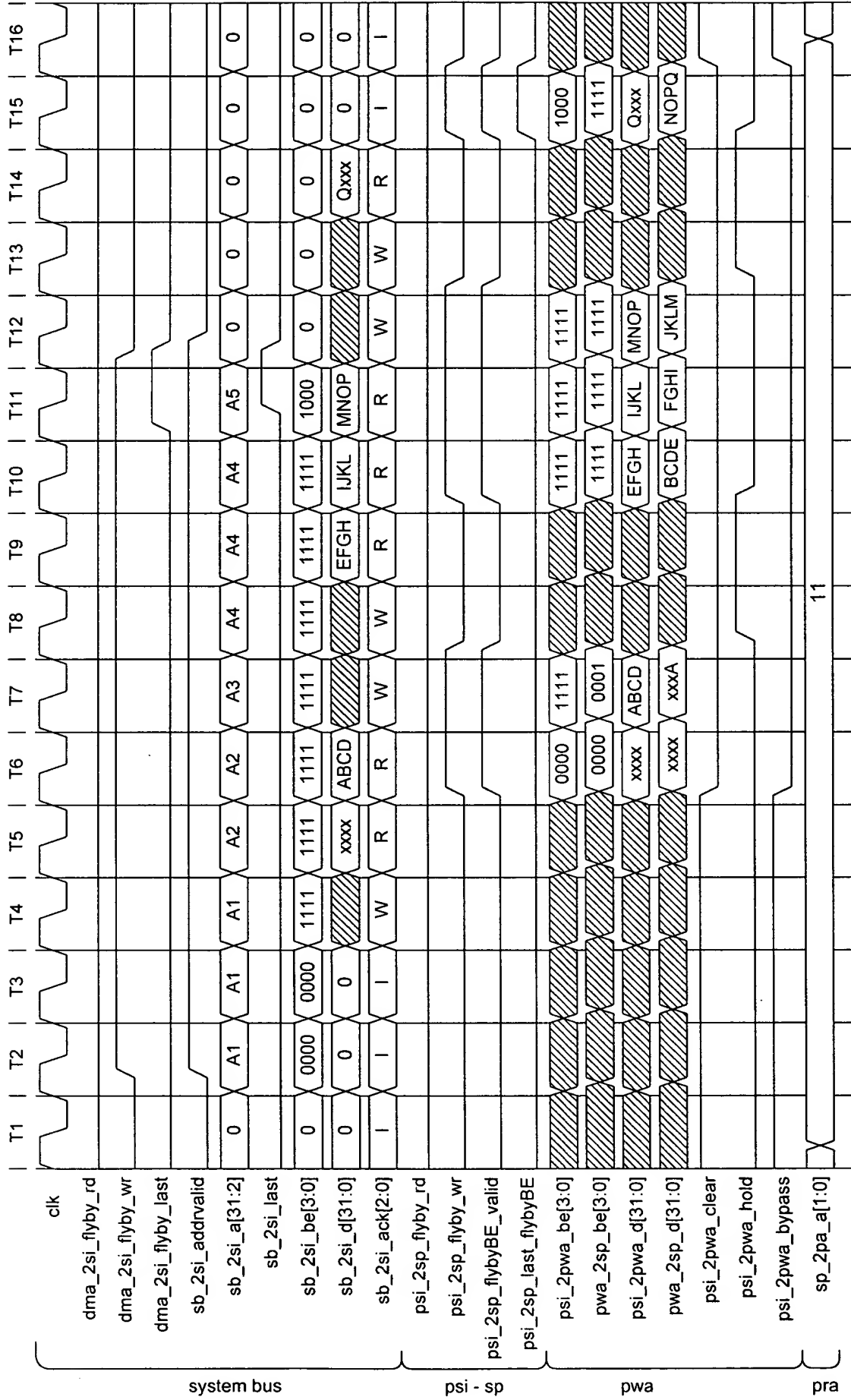


FIG. 9



FLY-BY READ (MEMORY CONTROL DEVICE 103)

FIG. 10



psi_2pra_hold = 0
 psi_2pra_load = 0
 psi_2pra_preload = 0
 psi_2pra_bypass = 1
 psi_2sb_d[31:0] = 0

FIG. 11

DATA IN MAIN MEMORY 104

ADDR	00	01	10	11
A1	x	A	B	C
A2	D	E	F	G
A3	H	I	J	K
A4	L	M	N	O
A5	P	Q	x	x
A6	x	x	x	x

FIG. 12

DATA, ADDRESS AND BYTE-ENABLES ON SYSTEM BUS 105

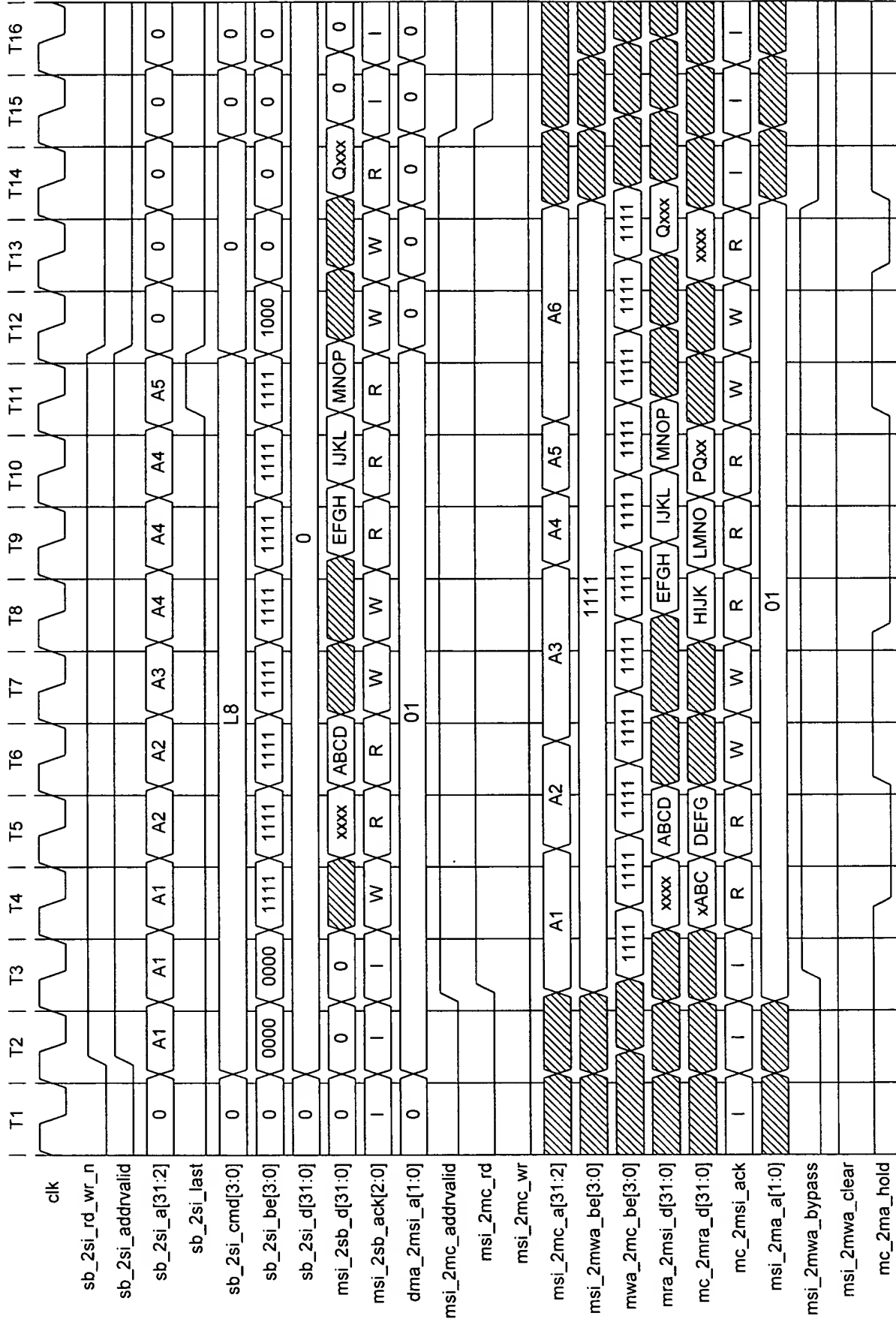
ADDR	00	01	10	11	BE
A1	x	x	x	x	0000
A1	A	B	C	D	1111
A2	E	F	G	H	1111
A3	I	J	K	L	1111
A4	M	N	O	P	1111
A5	Q	x	x	x	1000

FIG. 13

DATA AND BYTE ENABLES RECEIVED BY SLAVE PERIPHERAL 113

00	01	10	11	BE
x	x	x	x	0000
x	x	x	A	0001
B	C	D	E	1111
F	G	H	I	1111
J	K	L	M	1111
N	O	P	Q	1111

FIG. 14



FLY-BY WRITE (MEMORY CONTROL DEVICE 103)

FIG. 15